LOW VOLTAGE LOW POWER SIGNAL PROCESSING SYSTEM AND METHOD FOR HIGH ACCURACY PROCESSING OF DIFFERENTIAL SIGNAL INPUTS FROM A LOW POWER MEASURING INSTRUMENT

FIELD OF THE INVENTION

5   The present invention relates to low power electronic measuring instruments and, more particularly, to a low voltage low power signal processing system and method for high accuracy processing of differential signal inputs from sensors included in portable and/or low power measuring instruments such as electronic

10   calipers, linear or angular position gauges, tilt or level gauges, pressure gauges and the like.

BACKGROUND OF THE INVENTION

Various portable electronic measuring instruments are currently available. One example of such an instrument is a displacement measuring instrument, a hand-

15   held electronic caliper which can be used for making precise measurements of machined parts to ensure that they are meeting tolerance requirements. It is obvious that the less power such instruments use, the fewer batteries (or other power sources) they will require and the longer they will operate before the batteries (or other power sources) need to be replaced or replenished. However, reducing the power

20   requirements of such devices is a complex task. Such devices are required to make highly accurate measurements, and the complex signal processing techniques that

have been developed for such devices tend to complicate the process of designing circuitry that will both accomplish the desired accuracy and operate at low voltage and power levels.

An example of an electronic caliper using highly accurate measuring techniques is shown in U.S. Patent No. 5,901,458, which is commonly assigned and hereby incorporated by reference in its entirety. As described, the electronic caliper has a reduced offset position transducer that uses a read head that is movable along a scale. The electronics provide a precise measurement of the read head's position on the scale. The transducer uses two sets of coupling loops on the scale to inductively couple a transmitter winding on the read head on a slide to one or more receiver windings on the read head. The transmitter winding generates a primary magnetic field. The transmitter winding is inductively coupled to first loop portions of first and second sets of coupling loops by a magnetic field. Second loop portions of the first and second sets of coupling loops are interleaved and generate secondary magnetic fields. A receiver winding is formed in a periodic pattern of alternating polarity loops and is inductively coupled to the second loop portions of the first and second sets of coupling loops by the secondary magnetic fields. Depending on the relative position between the read head and the scale, each polarity loop of the receiver winding is inductively coupled to a second loop portion of either the first or second set of coupling loops. The relative positions of the first and second loop portions of the first and second sets of coupling loops are periodic and dependent on the relative position of the coupling loops on the scale.

Another example is shown in U.S. Patent No. 5,886,519, which is commonly assigned, and incorporated herein by reference in its entirety. The '519 patent discloses an inductive absolute position transducer for high accuracy applications, such as linear or rotary encoders, electronic calipers and the like. The absolute position transducer uses two members movable relative to each other. The first member contains at least one active transmitter for generating a magnetic field and at least one receiver for receiving the generated magnetic field. The passive second member includes passive flux modulating elements that modulate the received field

depending on their position relative to the at least one receiver. An electronic circuit coupled to the at least one transmitter and the at least one receiver compares the outputs of the at least one receiver, evaluates the absolute position between the two members, and exhibits the position on a display. The inductive absolute position

5 transducer determines the absolute position between the two members.

Systems such as those shown in the '458 and '519 patents utilize advanced signal processing techniques to produce highly accurate displacement measurements. The present invention is directed to a portable electronic measuring instruments, and especially to portable electronic displacement measuring instruments, that produces

10 highly accurate measurements while using a low voltage low power system.

SUMMARY OF THE INVENTION

The present invention provides a low voltage low power signal processing system and method for use in portable measuring instruments such as electronic calipers linear or angular gauges, level gauges, pressure gauges and the like. As part

15 of the low voltage low power system and method, a conversion process is performed such as an analog-to-digital conversion which utilizes a time-varying reference signal such as a ramp signal to produce timing measurements that are used to determine the digital outputs of the conversion.

The accuracy of the advanced transducers and signal processing methods that

20 are used in portable measuring instruments such as electronic calipers and the like is often dependent on producing a precisely linear conversion of the measured input quantity to a useful form of output, thus, it is desirable to avoid the production of second order distortion in such systems. Second order distortion can occur if differential signals are converted to single-ended signals, such as is done when using

25 conventional time-varying reference signal conversion methods. The present invention utilizes a time-varying reference signal method for the conversion processing and yet avoids the production of second order distortion by not converting the signals to a single-ended format, and instead providing circuitry for processing the signals as differential signals.

The system of the invention may be used with transducers which output multiple signals in parallel, for example in a three-phase transducer configuration. The preferred signal processing techniques for the three-phase configuration are able to cancel most of the third harmonic distortion in the system. Thus, the fully

5   differential circuits of the invention are advantageous in such systems because the third harmonic error cancellation inherent to the three-phase technology is perfectly complemented by the second harmonic error suppression of the fully differential circuits. These techniques minimize the distortion-related errors present in the final measurement values determined according to the systems and methods of this

10   invention, even with the limitations imposed by the low power and voltage supply requirements. Also, the techniques provide for simple circuits that minimize distortion-related errors.

In accordance with one aspect of the invention, the analog-to-digital converter is implemented as a parallel, single ramp, with two matched comparators for each leg

15   of differential input. Therefore, in an embodiment with a three-phase transducer, there would be six inputs from the three phases which would be provided to six comparators. One of the inputs of each of the comparators receives the differential signals, while the other input of each of the comparators receives the ramp signal.

The ramp analog-to-digital converter of the present invention can be

20   implemented with relatively simple circuitry, and consequently be of a small size and operable from low voltage. An operating speed limitation of the system is due to the nature of the ramp itself, since a ramp inherently takes time to transition. However, since high-speed operation is not a critical factor in the signal processing of a variety of portable or handheld measuring instruments (e.g., electronic calipers), this

25   implementation provides an effective tradeoff of a slower system for one that uses less power, is of a smaller size and is operable from low voltage. For the sampling speed of the many portable measuring systems, a primary consideration is making the samples frequent enough to avoid flickering on a display that can be detected by the human eye. In one embodiment, a sampling rate in excess of 10 samples per second

(thus having a processing time per sample of about 100 ms) is sufficient to address this consideration.

In accordance with another aspect of the invention, the analog-to-digital converter of the present invention may be used in a portable measuring instrument that is operable from a power supply providing a voltage less than 1.75 volts (e.g., a single 1.5 volt watch battery or solar cell), and has a current drain compatible with portable measuring instruments which require an overall current drain as low as 5 microamps. Thus, this embodiment would satisfy system requirements as low as 1.5 volts nominal (1.35 volts minimum). The system of the present invention minimizes the current drain and maximizes the dynamic range of the analog circuits by using fully differential circuits, powering them from the 1.5 volt source, and further may use NMOS switches with voltage boosters. The invention is also advantageous in systems with voltages higher than 1.5 volts, such as one that is operable from a power supply providing a voltage less than 3.5 volts (e.g., two 1.5 volt watch batteries or solar cells in series). The invention is also advantageous in some applications operating with voltages higher than 3.5 volts.

In accordance with another aspect of the invention, certain components are selected to reduce the sensitivity of the overall system to process parameters. More specifically, by using capacitors of the same type in the ramp generator and clock generator, and charging them with scaled bias currents, and by using resistors and capacitors of the same type in the clock and analog-to-digital converter, the scale factor of the system is made to be independent of process parameters, as well as later environmental effects due to operating temperature, circuit aging, and the like. In addition, since the transducer signal will be proportional to the supply voltage, by deriving the reference voltage directly from the power supply (using a divider), the system's scale factor (peak-to-peak counts for each phase signal) will be made to be independent of the supply voltage variations, whatever their cause.

In accordance with another aspect of the invention, the comparators may be implemented in any way suitable for low voltage low power operation. Either a low power operational amplifier-type comparator or a dynamic comparator may be used.

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Comparators having a switched capacitor input have the advantage of storing the input voltage on the input capacitor, which allows the preceding stage of the analog signal processing circuitry to be turned off, thereby saving power and facilitating cancellation of the comparator offset. In general, since the comparators are identical,

5 any delays and parasitic effects should not affect accuracy and the choice of the low voltage low power comparator design is not critical.

In accordance with another aspect of the invention, the counter that is used may be a ripple counter, which typically has a low current drain, since it minimizes the number of toggles. To minimize the number of registers, the count value is

10 stored in the counter itself. It should also be noted that no subtraction circuit is needed. The sign signal is stored in a separate register. The end result of these design choices is a highly efficient circuit, both in terms of small size, low voltage operation and low current drain.

The analog-to-digital converter of the present invention also has a number of

15 advantages with regard to the effects of leakage currents. One advantage is that the effect of leakage in the analog-to-digital converter comparators will be canceled, since the design is fully differential in nature. In addition, while voltage dependent leakage will introduce third order distortion, the third order distortion will not introduce position errors in the case of the above-described three-phase system.

20 Furthermore, mismatches in leakage will have the same effect as any other mismatch, such as offset and scale factor mismatches between channels. This should be quite small (second order effect) and can be canceled by error correction.

BRIEF DESCRIPTION OF THE DRAWINGS

The foregoing aspects and many of the attendant advantages of this invention

25 will become more readily appreciated as the same become better understood by reference to the following detailed description, when taken in conjunction with the accompanying drawings, wherein:

FIGURE 1 is a block diagram of a measurement system using a ramp analog-to-digital converter in accordance with the present invention;

FIGURE 2 is a block diagram of one embodiment of the measurement system of FIGURE 1 using multiple three-phase transducer windings;

FIGURE 3 is a schematic diagram illustrating one embodiment of connections for the three-phase windings illustrated in FIGURE 2;

5   FIGURE 4 is an output diagram of the three-phase windings of FIGURE 3 showing the signal amplitudes of the three-phases as a function of the relative position of the scale within the transducer;

FIGURE 5 is a schematic vector phase diagram for the three-phase windings of FIGURE 3;

10   FIGURE 6 is a block diagram of an embodiment of the ramp analog-to-digital converter of FIGURE 1;

FIGURE 7A is a graph illustrating possible second order distortion in a ramp signal used in a ramp analog-to-digital converter;

FIGURE 7B is a graph illustrating the possible symmetrical third order

15   distortion in a ramp analog-to-digital converter;

FIGURE 8 is a block diagram of one embodiment of a logic circuit for one of the differential channels of the analog-to-digital converter of FIGURE 6;

FIGURE 9A is a timing diagram illustrating the operation of the logic circuit of FIGURE 8 for a positive counter output value;

20   FIGURE 9B is a timing diagram illustrating the operation of the logic circuit of FIGURE 8 for a negative counter output value;

FIGURE 10 is a block diagram of the current generator of FIGURE 8;

FIGURE 11 is a block diagram of the clock generator of FIGURE 8;

FIGURE 12 is a timing diagram illustrating the operation of the clock

25   generator of FIGURE 11;

FIGURE 13 is a detailed schematic diagram of the clock generator of FIGURE 11;

FIGURE 14 is a system block diagram for the analog-to-digital converter of FIGURE 6 for a analog-to-digital converter having six fully-differential channels;

30   and

FIGURE 15 is a timing diagram illustrating the operation of the block diagram of FIGURE 14.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENT

FIGURE 1 shows a functional block diagram of a measurement system 8

5   using a ramp analog-to-digital converter 80 in accordance with the present invention. The ramp analog-to-digital converter 80 will be described in more detail below with reference to FIGURE 6. In short, the ramp analog-to-digital converter provides a low voltage low power implementation that is able to produce highly accurate differential signal measurements.

10   As also shown in FIGURE 1, the measurement system 8 includes a multi-signal transducer and driver/receiver circuitry 10, which outputs analog differential signals on signal lines 10A and 10B to the analog signal processor 70. The analog signal processor 70 outputs differential signals on signal lines 70A and 70B to the ramp analog-to-digital converter 80. As will be described in more detail below, the

15   differential nature of the output signals is an important consideration in the design of the analog-to-digital converter 80. In summary, the use of the differential signals avoids the production of additional second order distortion which is commonly associated with single-ended signal processing of transducer output signals. Third order distortion is thus the primary distortion in the system. As will be described in

20   more detail below, in various exemplary embodiments, signal processing techniques can then be used to cancel much of the third harmonic distortion from the system.

In conventional systems single-ended signals are typically used with low voltage low power analog-to-digital converters such as ramp converters. However, as will be described in more detail below, the conversion of the differential signals

25   into single-ended signals typically produces significant amounts of second order distortion in the system. The introduction of second order distortion significantly reduces the accuracy of measuring systems. The method by which the ramp analog-to-digital converter 80 of the present invention processes the differential signals from the analog signal processor 70, and thus avoids the need to convert the signals to a

30   single-ended format, will be described in more detail below with reference to

FIGURE 6. It should be appreciated that, in the prior art, many of the circuit design and accuracy problems mentioned previously, and discussed in greater detail further below, have been conventionally solved by adding circuit complexity. However, such conventional solutions are incompatible with the particularly low power low

5   voltage operating requirements of a variety of portable and handheld measuring instruments. Thus, the reader should appreciate that the simplicity and other features of the design elements of the present invention, each separately and also together, provide particular benefit for highly accurate transducer signal processing in combination with the particularly low power low voltage operating requirements of a

10   variety of portable and handheld measuring instruments.

The ramp analog-to-digital converter 80 outputs digital values over a data line 80A to a logic circuitry 90. Logic circuitry 90 provides and receives signals from a control unit 60 over a data and power bus 90A. In one embodiment, logic circuitry 90 comprises a hard wired logic circuit, as will be described in more detail

15   below with reference to FIGURE 8. However, it will be understood that the logic circuitry 90 could consist of a microprocessor, or any implementation of a suitable finite state machine as is known in the art. The control unit 60 also provides control signals over a data and power bus 60A to the multi-signal transducer and driver/receiver circuitry 10, control signals over a data and power bus 60B to the

20   analog signal processor 70, and control signals over a data and power bus 60C to the ramp analog-to-digital converter 80. A low voltage power supply 50, may supply power to the entire measurement system 8 through one or more power lines 50A, the power further distributed through the various data and power buses of the system, and subject to the control of the digital control unit 60.

25   While FIGURE 1 shows a functional block diagram for the measurement system 8, it will be appreciated that the measurement system 8 is presented as an exemplary embodiment. The low power low voltage systems and methods of this invention may be implemented in conjunction with a variety of transducer systems or other appropriate known or later developed precision measuring systems.

30   Furthermore, it will be appreciated that the transducer in circuitry 10 may be

implemented using any appropriate known or later developed multi-signal transducer, including, for example, the transducers disclosed in the incorporated '458 and '519 patents.

FIGURE 2 shows a block diagram of one embodiment of the measurement system of FIGURE 1, in which multiple three-phase transducer windings are used. FIGURE 2 shows an example of a three-scale track design, where there are three sets of three-phase receiver windings. This three-scale track design is described in more detail in copending U.S. Patent Application Serial No. 09/268,674, which is commonly assigned and hereby incorporated by reference in its entirety.

As shown in FIGURE 2, the measurement system 108 includes a transmitter winding 122 that is connected to a transmitter driver circuit 152. The transmitter winding 122 is indirectly inductively coupled via coupling loops formed on a scale member of the induced current position transducer to the first, second, and third receiver windings 124, 126 and 127, which are connected to a multiplexer 155. The differential output of the multiplexer 155 is connected through lines 155A and 155B to an analog signal processor 170. The differential output of the analog signal processor 170 is provided on six output lines 170A to 170F to the input of an analog-to-digital converter 180. The analog-to-digital converter 180 converts the differential output of the analog signal processor 170 from an analog signal to a digital signal. The digital signal from the analog-to-digital converter 180 is output on a line 180A to a logic circuitry 190, which processes the digital signal from the analog-to-digital converter 180 to determine the relative position between the read head and the scale member 110.

Each position within a wavelength can be uniquely identified by the logic circuitry 190 according to known techniques and equations disclosed in the incorporated '458 and '519 patents. The logic circuitry 190 also controls the sequence of signal sampling by outputting a control signal over signal lines 190A-190D to a digital control unit 160. The digital control unit 160 controls the sequence of transmission, signal sampling and analog-to-digital conversion by outputting control signals on the power and signal bus lines 160A-160D to the transmitter

drivers 152-154, multiplexer 155, the analog signal processor 170 and the ramp analog-to-digital converter 180.

In particular, as shown in FIGURE 2, the digital control unit 160 outputs control signals over the power and signal bus lines 160A-160C to the transmitter drivers 152-154, respectively, to controllably excite the transmitter windings. The digital control unit 160 also outputs switch and control signals on the power and signal bus lines 160D-160F to the multiplexer 155. The control signals on lines 160D-160F determine which of the possible phases of the multi-scale-track, multi-phase receiver windings 124, 126 and 127 is input to the analog signal processing circuits 170 that follow the multiplexer 155. A low voltage power supply 150, may supply power to the entire measurement system 108 through one or more power lines 150A, the power further distributed through the various data and power buses of the system, and subject to the control of the digital control unit 160.

As noted above, FIGURE 2 shows an example of a three-scale track design, where there are three sets of three-phase receiver windings. The multiplexer 155 will choose one signal, or in the case of differential measurements, one signal pair, to be output to the analog signal processor 170. The chosen signal, or signal pair, is then processed by the analog signal processor 170. The output of the analog signal processor 170 is provided on signal lines 170A-170F, which are input to analog-to-digital converter 180. The logic circuitry 190 can access the output of the analog-to-digital converter 180. Furthermore, because the logic circuitry 190 controls the operation of the digital control unit 160, the logic circuitry 190 can choose to select the scale tracks or phases in any sequential order.

As described in more detail in the incorporated '674 application, the above embodiment that describes signal multiplexing between the multiple phases of a single set of receivers will also apply equally well to the multiplexing between the multiple phases of two or more sets of multi-phase receivers. For example, in a three-scale track system as shown in FIGURE 2, the input multiplexer 155 can choose between 9 possible phase pairs to process. To cancel certain circuit errors, it can also choose these phase pairs in a reverse polarity mode that effectively inverts

the signal. Thus there are in total 18 possible ways to process the 9 phase pairs of a three-scale-track, three-phase system.

FIGURE 3 shows a schematic diagram illustrating one possible set of interconnections for one of the three-phase windings of FIGURE 2. As illustrated,

5 the three windings 218, 220 and 222, each have their lower portions connected to a common node. In the diagram of FIGURE 3, the common node is shown to be connected to a reference voltage V_{COMMON}, which in various exemplary embodiments may be set at a voltage level suitable for biasing the input of one or more amplifiers in an analog signal processor which receives signals from the three-

10 phase windings 218, 220 and 222. As also shown in FIGURE 3, a primary winding 210 is located on the other side of a scale 204 from the three-phase windings 218, 220 and 222. In a physical layout, the three-phase windings 218, 220 and 222 are offset from each other along the measurement axis by 1/3 of a wavelength λ.

15 FIGURE 4 shows the amplitudes of the signal from the three receivers, which are sinusoidal as a function of the position along the measurement axis. It will be appreciated that perfectly sinusoidal output functions of FIGURE 4 are difficult to achieve in practice, and that deviations from a perfect sinusoidal output contain spatial harmonics of the fundamental wavelength of the transducer. Such spatial

20 harmonics are significant not only in systems such as the measurement system 108, but also in the output signals of nearly all multi-signal displacement transducers such as linear and rotary optical encoders, resolvers, synchro's, INDUCTOSYN® displacement transducers, and the like. Such spatial harmonics are a limiting factor in the accuracy of many such devices, and precise devices often incorporate special

25 design features to reduce or eliminate these harmonics. Therefore, the three-phase configuration of this embodiment of the induced current position transducer has a significant advantage over other embodiments of the transducer in that the third harmonic content in the separate receiver windings' signal can be largely eliminated as a source of position measurement error.

Eliminating the third harmonic may be accomplished, for example, by combining the outputs of the receiver windings as shown in FIGURE 5, where the three windings are connected in a star configuration and the signals used for determining position are taken between the corners of the star. The following equations outline how the third harmonic component is eliminated by suitably combining the original three-phase signals, designated as U_R, U_S, and U_T.

Assume each of the unprocessed phase signals contains the fundamental sinusoidal signal plus the third harmonic signal, with equal amplitude in the three-phases, then:

$$U_R = A_0 \sin\left(2\pi \frac{x}{\lambda}\right) + A_3 \sin\left(2\pi \frac{3x}{\lambda}\right)$$

$$U_S = A_0 \sin\left(2\pi \frac{x + \frac{\lambda}{3}}{\lambda}\right) + A_3 \sin\left(2\pi \frac{3\left(x + \frac{\lambda}{3}\right)}{\lambda}\right)$$

$$= A_0 \sin\left(2\pi \frac{x}{\lambda} + \frac{2\pi}{3}\right) + A_3 \sin\left(2\pi \frac{3x}{\lambda} + 2\pi\right)$$

$$= A_0 \sin\left(2\pi \frac{x}{\lambda} + \frac{2\pi}{3}\right) + A_3 \sin\left(2\pi \frac{3x}{\lambda}\right)$$

$$U_T = A_0 \sin\left(2\pi \frac{x - \frac{\lambda}{3}}{\lambda}\right) + A_3 \sin\left(2\pi \frac{3\left(x - \frac{\lambda}{3}\right)}{\lambda}\right)$$

$$= A_0 \sin\left(2\pi \frac{x}{\lambda} - \frac{2\pi}{3}\right) + A_3 \sin\left(2\pi \frac{3x}{\lambda} - 2\pi\right)$$

$$= A_0 \sin\left(2\pi \frac{x}{\lambda} - \frac{2\pi}{3}\right) + A_3 \sin\left(2\pi \frac{3x}{\lambda}\right)$$

When operations are performed to properly pair-wise-subtract the above-outlined signals from each other, such operations can eliminate the third harmonic from the resulting signal, as indicated by the following equations:

$$V_R = U_T - U_S = A_0\left(\sin\left(2\pi\frac{x}{\lambda} - \frac{2\pi}{s}\right) - \sin\left(2\pi\frac{x}{\lambda} + \frac{2\pi}{3}\right)\right) = -A_0\sqrt{3}\cos 2\pi\frac{x}{\lambda} \qquad \text{Eq. 1}$$

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$$V_S = U_R - U_T = A_0\left(\sin\left(2\pi\frac{x}{\lambda}\right) - \sin\left(2\pi\frac{x}{\lambda} - \frac{2\pi}{3}\right)\right) = A_0\sqrt{3}\cos\left(2\pi\frac{x}{\lambda} - \frac{2\pi}{6}\right) \qquad \text{Eq. 2}$$

$$V_T = U_S - U_R = A_0\left(\sin\left(2\pi\frac{x}{\lambda} - \frac{2\pi}{3}\right) - \sin\left(2\pi\frac{x}{\lambda}\right)\right) = A_0\sqrt{3}\cos\left(2\pi\frac{x}{\lambda} + \frac{2\pi}{6}\right) \qquad \text{Eq. 3}$$

Operations corresponding to the preceding equations can be performed using the present invention, by taking differential signal measurements between

10 appropriate pairs of the signals U_R, U_S and U_T, to determine the signal values of V_R, V_S and V_T. Thus, the present invention is particularly useful for suppression of common-mode third harmonic content in the differential input signals, as described in greater detail below.

FIGURE 6 shows a block diagram of an exemplary embodiment of an

15 analog-to-digital converter formed in accordance with the present invention. As shown, the signals input to the exemplary analog-to-digital converter 300 are designated as differential inputs Ph0+ and Ph0-, differential inputs Ph1+ and Ph1-, and differential inputs Ph2+ and Ph2-. As illustrated in FIGURE 6, the analog-to-digital converter 300 is implemented as a parallel, differential input, single ramp

20 converter with two matched comparators for each leg of differential input. Therefore, the six inputs from the three phases are provided to six comparators 301 to 306. Each of the inputs Ph0+, Ph0-, Ph1+, Ph1-, Ph2+, Ph2- is provided to the positive input of one of the comparators 301, 302, 303, 304, 305, and 306, respectively. The negative inputs of each of the comparators 301 to 306 is provided

25 from the ramp generator 310. The specific operation of the ramp generator 310

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relative to the ramp analog-to-digital converter 300 will be described in more detail below with reference to FIGURES 8 and 9.

The outputs of the six comparators 301 to 306 are provided to three logic/counter circuits 330 to 332. More specifically, the outputs of the comparators 301 and 302 are provided to the logic counter 330, while the outputs of the comparators 303 and 304 are provided to the logic counter 331, and the outputs of the comparators 305 and 306 are provided to the logic counter 332. A temporary clock 320 also provides an input to each of the logic counters 330, 331, and 332. One or more of the logic/counter circuits 330-332 together with the temporary clock 320 operates to provide a digital differential value determining circuit. Logic counter 330 provides an output signal $Ph0_{out}$ while logic counter 331 provides an output signal $Ph1_{out}$, and logic counter 332 provides an output signal $Ph2_{out}$. Each of the logic/counter outputs is equal to the positive counter output minus the negative counter output, thus the output $Ph0_{out}$ is equal to [CNT0+] - [CNT0-], while the output $Ph1_{out}$ is equal to [CNT1+] - [CNT1-], and the output $Ph2_{out}$ is equal to [CNT2+] - [CNT2-].

As previously discussed, the systems and methods of this invention are particularly useful for suppression of common-mode third harmonic content in the differential input signals. In one embodiment of a system which illustrates this utility, with reference to FIGURE 5, each of the three outputs (U_S, U_T and U_R) of the three-phase windings is provided as two of the input signals to the exemplary analog-to-digital converter 300 of FIGURE 6. In particular, the output U_S is provided as both the negative differential input Ph0- and the positive differential input Ph1+, while the output U_T is provided as both the negative differential input Ph1- and the positive differential input Ph2+, while the output U_R is provided as both the negative input Ph2- and the positive input Ph0+.

With reference to the previously discussed equations Eq. 1-3, it should be appreciated that when the signal U_S is provided as both the negative differential input Ph0- and the positive differential input Ph1+, and the signal U_T is provided as both the negative differential input Ph1- and the positive differential input Ph2+, and the

signal U_R is provided as both the negative differential input Ph2- and the positive differential input Ph0+, then the output $Ph0_{out}$ corresponds to V_R, while the output $Ph1_{out}$ is corresponds to V_S, and the output $Ph2_{out}$ corresponds to V_T . Thus, it should be appreciated that exemplary analog-to-digital converter 300 is generally

5   useful for suppression of common-mode harmonic content in the differential input signals, and particularly useful for the suppression of third-order spatial harmonic content in differential input signals which are output by three-phase displacement transducers such as encoders, resolvers, and the like.

As described above, the signal processing techniques using fully differential

10   circuits are able to cancel the common-mode third harmonic distortion in an attached system which provides the differential inputs. These techniques allow the accuracy of measurements made using circuits according to the systems and methods of this invention to be maximized, even though the circuit is operated according to the limited voltage and power supply requirements of a variety of portable and handheld

15   instruments. As will be described in more detail below, it is a goal of the present invention to implement a low power low voltage system that works with and maintains the advantages of differential measurement, and that can furthermore acquire multiple differential signals in parallel, such as may be needed for the exemplary three-phase transducer configuration described above. The analog-to-

20   digital converter of the present invention is designed toward that end.

In one application, the analog-to-digital converter of the present invention may be used in a handheld displacement measuring device that operates from a single 1.5 volt watch battery or solar cell, and which has total measuring instrument current drain as low as 5 microamps. Thus, the analog-to-digital converter of the present

25   invention is operable from a single 1.5 volt watch battery or solar cell and draws current which is a fraction of 5 microamps . For reasons that will be described in more detail below, in the systems and methods of the present invention minimize the current drain and maximize the dynamic range of the included analog circuits by using fully differential circuits, powering them from a 1.5 volt source, and further

30   may use NMOS switches with voltage boosters.

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The ramp analog-to-digital converter of FIGURE 6 can be implemented with relatively simple circuitry, and consequently be of a small size. Small size is an advantage regarding the cost and packaging size required for the present invention. An operating speed limitation of the system is due to the nature of the ramp itself,

5   since a ramp inherently takes time to transition. However, since high-speed operation is not a critical factor in the signal processing of a variety of portable or handheld measuring instruments (e.g., electronic calipers), this implementation provides an effective tradeoff of a slower system for one that uses less power, is of a smaller size and is operable from low voltage. For the sampling speed of the many

10   portable measuring systems, a primary consideration is making the samples frequent enough to avoid flickering on the display that can be detected by the human eye. In one embodiment, a sampling rate of about 10 samples per second (thus having a processing time per sample of about 100 ms) is sufficient to address this consideration.

15   As illustrated in FIGURE 6, in one embodiment the present invention is implemented as a parallel, single ramp analog-to-digital converter with two comparators per differential-pair channel (one for each signal of the differential signal pair.) In this implementation, the scale factor matches perfectly for all three phases. Furthermore, in this implementation the analog-to-digital converter can be

20   extended to process two scales simultaneously. As will be discussed in more detail below, to limit the size of the charging capacitor of the charging circuit in the ramp generator, a temporary high-speed clock is used during conversion. A 1 megahertz clock gives an effective 12 bit resolution in a 2.048 millisecond (2048 counts times 2) implementation.

25   The implementation of FIGURE 6 also allows differential signals to be processed in parallel, and even multiple sets of differential signals. This provides distinct advantages over systems which attempt to convert the fully differential output to single-ended signals, since such processing will typically introduce unwanted second harmonic distortion. Second order distortion in this type of system

30   can produce significant measurement errors in a variety of applications. For

example, if the signals V_R, V_S, and V_T of equations Eq. 1-3 contain second harmonic distortion (not shown in equations Eq. 1-3) due to signal processing, then displacement calculations based on V_R, V_S, and V_T will be in error. Therefore, the introduction of second order distortion is extremely undesirable. The present

5   invention provides a way to process the signals as differential signals rather than single-ended signals, such that the production of undesirable second order distortion is avoided.

FIGURE 7A shows a graph of a second order distortion that may occur in a typical ramp signal. As illustrated, for a low voltage chip the ramp signal may have

10   some distortion, as the dynamic range is limited. FIGURE 7B is a graph showing the symmetrical third order distortion that may occur in an analog-to-digital converter according to the present invention using such a ramp. Since the analog-to-digital converter of the present invention is fully differential, the second order distortion is effectively transformed into a third order distortion nonlinearity of the form shown.

15   Circuits according to the systems and methods of this invention are advantageous in many important applications because signal distortion of the second harmonic type is essentially avoided, while the limited third harmonic type signal distortion that is introduced by the circuit is easily eliminated by subsequent signal processing. For example, returning to the previous discussion of a system where

20   each of the three outputs (U_S, U_T, and U_R) of the three-phase windings of FIGURE 3 is provided as two of the input signals to the exemplary analog-to-digital converter 300 of FIGURE 6 and the output PhO$_{out}$ corresponds to V_R, while the output Ph1$_{out}$ corresponds to V_R, and the output Ph2$_{out}$ corresponds to V_T, let us now assume that the signals V_R, V_S, and V_T of equations Eq. 1-3 each contain a

25   previously unconsidered common-mode third harmonic distortion newly introduced by the signal processing circuitry of the exemplary analog to digital converter 300. Such distortion is represented in the following equations, where the term a_3 is the amplitude of the third harmonic distortion:

$$V_{R-distort} = V_R + a_3 \cos\left(2\pi \cdot \frac{3x}{\lambda}\right)$$

Eq. 4

$$V_{S-distort} = V_S - a_3 \cos\left(2\pi \cdot 3\left(\frac{x}{\lambda} - \frac{1}{6}\right)\right) = V_S - a_3 \cos\left(2\pi \cdot \frac{3x}{\lambda} - \pi\right)$$

5   Eq. 5

$$V_{T-distort} = V_T - a_3 \cos\left(2\pi \cdot 3\left(\frac{x}{\lambda} + \frac{1}{6}\right)\right) = V_S - a_3 \cos\left(2\pi \cdot \frac{3x}{\lambda} + \pi\right)$$

Eq. 6

10   Fortuitously, in applications where a displacement is determined from three-phase signals such as V_R , V_R , and V_T , it is either convenient or necessary perform operations which derive quadrature signals from the three phase signals, that is, signals which bear the relationship of sine and cosine.   Such signals may be determined as follows:

15

$$Q_{SINE} = \frac{1}{\sqrt{3}}\left(V_{S-distort} - V_{T-distort}\right)$$

Eq. 7

$$= \frac{1}{\sqrt{3}}\left[V_S - V_T - a_3\left[\cos\left(2\pi \cdot \frac{3x}{\lambda} - \pi\right) - \cos\left(2\pi \cdot \frac{3x}{\lambda} + \pi\right)\right]\right]$$

20   Eq. 8

$$= \frac{1}{\sqrt{3}}\left[V_S - V_T\right]$$

Eq. 9

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$$Q_{COSINE} = -\frac{1}{\sqrt{3}}\left(2V_{R\cdot distort} - V_{S\cdot distort} - V_{T\cdot distort}\right)$$

Eq. 10

5 $$= -\frac{1}{\sqrt{3}}\left[2V_R - V_S - V_T + a_3\left[2\cos\left(\frac{6\pi x}{\lambda}\right) + \cos\left(\frac{6\pi x}{\lambda} - \pi\right) + \cos\left(\frac{6\pi x}{\lambda} + \pi\right)\right]\right]$$

Eq. 11

$$= -\frac{1}{3}\left[2V_R - V_S - V_T\right]$$

Eq. 12

10   It should be appreciated that the distortion terms associated with third harmonic signal processing distortion have been eliminated by the operations of equations Eq. 7-12 and displacements calculated based on the results of equations Eq. 7-12 will thus be free of common-mode third harmonic errors introduced by signal processing. Thus, it should be further appreciated that the particular

15   combination of signal processing characteristics associated with the present invention are of particular advantage in a number of applications of circuits according to the systems and methods of this invention where signal processing or calculations may be used to remove common-mode third harmonic signal distortion, and more

20   particularly in those applications where displacement determinations are calculated based on three-phase transducer signals.

       FIGURE 8 is a block diagram of a logic circuit 400 illustrating the processing for one of the three phases of the analog-to-digital converter 300 of FIGURE 6. The comparators 401 and 402 represent a pair of the comparators 301 to 306, and the

25   input signals IN+ and IN- represent the positive and negative portions of one of the phase signals Ph0, Ph1, or Ph2. The signal RAMP is provided to the negative inputs of each of the comparators 401 and 402. The signal RAMP is provided by a current generator 410, which will be discussed in more detail below with reference to

FIGURE 10. The inputs to current generator 410 are the reference signal V_{REF} and the signal ON. The reference signal V_{REF} controls the current generator 410 and thus the ramp current and therefore the scale factor. In various exemplary embodiments, V_{REF} is derived directly from the overall system power supply (using a divider), and the overall measurement system's scale factor (peak-to-peak counts for each signal derived from a transducer) is thereby made to be independent of the system supply voltage variations, as will be described in more detail below. In one 1.5V system embodiment, the reference signal V_{REF} is at 0.75V, or one half of the power supply voltage.

A capacitor C_R is coupled between the output of the current generator 410 and ground. A switch SW1 is controlled by control signal RST to couple the signal RAMP to a signal REFL. The signal RAMP is reset to the signal REFL, which is selected to be the lowest end of the input signal range, rather than ground in order to save time (and current). In one 1.5V system embodiment, with a signal range of 750 mV maximum (600 mV nominal), the signal REFL is set at approximately 375 mV.

The output signal CMP+ of comparator 401 is provided as both an input to an exclusive OR 430 gate and as an input to a DFF block 460. Similarly, the output signal CMP- of the comparator 402 is provided as an input to the exclusive OR gate 430 as well as an input to the DFF block 460. The output signal COUNT of the exclusive OR gate 430 is provided as an input to an AND gate 440. A second input of the AND gate 440 is a signal CLK received from a clock generator 420. Clock generator 420 receives the input signal ON. The clock generator 420 will be discussed in more detail below with reference to FIGURE 11. The output of the AND gate 440 is provided to an 11 bit counter 450. The output of the counter 450 is the signal OUT. The output of the DFF block 460 is the signal SIGN. The signal SIGN adds an additional bit to the 11 bit output of the counter 450, thus creating an overall output of 12 bits of the logic circuit 400.

It will be appreciated that the logic current 400 of FIGURE 8 is merely shown as an exemplary embodiment. One particular design choice is either to use one

counter for each phase, or one counter with two sets of registers for each phase. The optimum approach will depend on the size and current consumption requirements. In general, the current drain is often dominated by the oscillator and the counter(s).

In the particular embodiment of the logic circuit 400 of FIGURE 8, the
5 counter 450 may be a ripple counter, which typically has a low current drain, since it minimizes the number of toggles. To minimize the number of registers, the count value is stored in the counter itself. It should also be noted that no subtraction circuit is needed. The sign signal SIGN is stored in a separate register. The end result of these design choices is a highly efficient circuit, both in terms of small size and low
10 current drain. However, it will be appreciated that this is merely an exemplary embodiment and that other design choices may obviously be made.

Also in the embodiment of the logic circuit 400 of FIGURE 8, the comparators may be implemented in any way suitable for low voltage low power operation. Either a low power operational amplifier-type comparator or a dynamic
15 comparator may be used. The reader is referred to the chapter titled "Comparators" in *Analog Integrated Circuit Design* by David Johns and Ken Martin, published by John Wiley and Sons, Inc., 1997. Comparators having a switched capacitor input have the advantage of storing the input voltage on the input capacitor, which allows the preceding stage of the analog signal processing circuitry to be turned off, thereby
20 saving power and facilitating cancellation of the comparator offset. In an embodiment using comparators having an internal switched capacitor input, the capacitor is preferably internally switchably connected to the input signal input during a reset phase, and just prior to conversion of an input signal, the input signal input is switchably disconnected and the ramp signal is switchably connected to the
25 capacitor input at the start of the input signal conversion.. In general, since the comparators are identical, any delays and parasitic effects should not affect accuracy and the choice of the low voltage low power comparator design is not critical.

FIGURES 9A and 9B are timing diagrams illustrating the operation of the logic circuit 400 of FIGURE 8. FIGURE 9A illustrates an example of a positive

counter output value, while FIGURE 9B illustrates an example of a negative counter output value.

As illustrated in FIGURE 9A, at a time T0 all of the signals are low. At a time T1, the signal ON transitions high, as does the signal RST. With reference to

5   FIGURE 8, the signal ON activates the current generator 410 and clock generator 420. The signal RST closes the switch SW1 so as to tie the output of the current generator 410 and consequently the signal RAMP to the signal level REFL. Thus, the signal RAMP rises to the signal level REFL.

At a time T2, the signal RST transitions low. With reference to FIGURE 8,

10   this opens the switch SW1 and allows the signal RAMP to increase at a linear rate as driven by the current generator 410. At a time T3, the signal RAMP passes the level of the input signal IN- of the comparator 402, and the output signal CMP- of the comparator 402 transitions high. This transition also causes the output COUNT of the exclusive OR gate 430 to transition high. This sequence, in combination with the

15   clock generator output signal CLK, causes the counter 450 to start to count.

At a time T4, the signal RAMP passes the level of the input signal IN+ of the comparator 401. This causes the output of the comparator 401 to transition high, thus causing the output COUNT of the exclusive OR gate 430 to transition low, which through the AND gate 440 causes the counter 450 to stop counting. At a time

20   T5, the signal ON transitions low and the signal RAMP stops increasing.

As described above, the sequence shown in FIGURE 9A causes the counter 450 to produce a digital value that is representative of the difference between the analog levels of the signals IN+ and IN-. The fact that the signal SIGN from the output of the DFF block 460 remains low, indicates that the digital output represents

25   a positive counter output value. This method provides a way to achieve a digital output of the difference between two differential analog signals.

FIGURE 9B is similar to FIGURE 9A except that it illustrates the function of the circuit for a negative counter output value. All of the signal levels are the same as in FIGURE 9A, except that the levels of the signals IN+ and IN- have been

30   swapped. Thus, at time T3, the signal RAMP passes the level of the signal IN+, thus

causing the output CMP+ of the comparator 401 to transition high and start the
counter 450. At time T4, the signal RAMP passes the level of the signal IN+, thus
causing the output of CMP+ of the comparator 401 to transition high. This causes
the output COUNT of the exclusive OR gate 430 to transition low, and stops the

5   counter 450. One important difference between FIGURES 9A and 9B is that at time
T4, in FIGURE 9B, the output SIGN of the DFF block 460 transitions high. The
signal SIGN being high provides an indication to the logic circuitry that the digital
value from the counter 450 represents a negative counter output value.

FIGURES 10 and 11 are block diagrams of the current generator 410 and

10   clock generator 420, respectively, of FIGURE 8. With regard to the design of these
circuits, certain components are selected to reduce the sensitivity of the overall
system to process parameters. More specifically, by using capacitors of the same
type in the ramp generator and clock generator, and charging them with scaled bias
currents, the scale factor of the system is made to be independent of process

15   parameters.

FIGURE 10 shows a block diagram of the current generator 410 of
FIGURE 8 for generating the ADC ramp signal. An operational amplifier 510
receives the reference signal V_{REF} at its positive input. The output of the
amplifier 510 is provided to a current mirror 512. Current mirror 512 also receives

20   power supply voltage VDD. The current mirror 512 is coupled through a resistor R_R
to ground, and the node between the resistor R_R and the current mirror 512 is also
coupled to the negative input of the amplifier 510. The output OUT of the current
mirror 512 provides a current level equal to I_{R1}, which mirrors the current I_R which
passes through the resistor R_R. The output OUT from the current mirror 512 is

25   coupled to the capacitor. The output OUT is also coupled through a switch SW5 to
the reference signal REFL. The output signal OUT provides the ramp signal RAMP.

FIGURE 11 is a block diagram of one exemplary embodiment of the clock
generator 420 of FIGURE 8. As shown, a current mirror 520 is coupled in its first
branch through a resistor R_{C1} to the power supply voltage VDD and a current i_{c1} is

30   established in the current mirror. The node between the resistor R_{C1} and the first

branch of the current mirror 520 determines the signal $V_{TH} = VDD - (R_{C1} * i_{C1})$.
The resistor R_{C1} and the first branch of the current mirror 520 form a current setting circuit 515. The second branch of the current mirror 520 is coupled to the positive input of a comparator 530. A signal RAMP1 is designated as the signal at the positive input of the comparator 530. The positive input of the comparator 530 is also coupled through a switch SW3 to the power supply voltage VDD. Switch SW3 is controlled by a signal SIG3 from a logic circuit 550. The positive input of the comparator 530 is also coupled through a capacitor C_{C2} to ground. The components switch SW3, capacitor C_{C2}, and second branch of the current mirror 520 all form a ramp circuit 525. The negative input of the comparator 530 receives a voltage signal V_{TH}. The output of the comparator 530 is provided to the logic circuit 550.

The output of a comparator 540 is also provided to the logic circuit 550. Similar to the comparator 530, the comparator 540 receives the voltage signal V_{TH} at its negative input. The positive input of the comparator 540 is coupled through a capacitor C_{C4} to ground. A current source 560 is also coupled to the positive input of the comparator 540. A switch SW4 also couples the positive input of the comparator 540 to the power supply voltage VDD. Switch SW4 is controlled by a control signal SIG4 from the logic circuit 550. The signal on the positive input of the comparator 540 is designated as signal RAMP2. The output of the logic circuit 550 is the clock signal CLK. The components switch SW4, capacitor C_{C4}, and current source 560 form a ramp circuit 535.

FIGURE 12 shows timing diagrams illustrating the operation of the clock generator 420 of FIGURE 11. As illustrated, at a time T0 both the signals RAMP1 and RAMP2 are high, and the clock signal CLK is low. At a time T1, the clock signal CLK transitions high, which causes the ramp signal RAMP1 to begin transitioning downward from the power supply voltage VDD at a linear slope. At a time T2, the ramp signal RAMP1 reaches the signal level V_{TH}, which causes the output 530A of the comparator 530 to transition. The transitioning of the output 530A causes the logic circuit 550 to transition. The logic circuit 550 thus transitions the clock signal CLK low at time T2. This also causes the logic

circuit 550 to transition the signal SIG3 so as to close the switch SW3 and tie the signal RAMP1 to the power supply voltage VDD. The signal SIG4 is also transitioned so as to open a switch SW4, thus allowing the signal RAMP2 to begin transitioning downward from the power supply voltage VDD at a linear slope.

5   At a time T3, the signal RAMP2 reaches the voltage level V_{TH}, thus causing the comparator 540 to transition. The transitioning of the output 540A of the comparator 540 causes the logic circuit 550 to transition its output signals. Therefore, the logic circuit 550 transitions the control signal SIG3 low, the control signal SIG4 high, and the clock signal CLK high. The transitioning of the control signal SIG3 low opens the switch SW3, thus allowing the signal RAMP1 at the input of the comparator 530 to begin transitioning downward at a linear slope. The transitioning of the signal SIG4 high closes the switch SW4, thus tying the signal RAMP2 at the positive input of the comparator 540 to the power supply voltage VDD.

15   At time T4, the process repeats similar to what occurred at time T2. Thus, the signal RAMP1 transitions to the power supply voltage VDD as switch SW3 is closed, and the signal RAMP2 begins transitioning downward at a linear slope as the switch SW4 is opened. The clock signal CLK also transitions low.

      FIGURE 13 is a detailed schematic diagram of one exemplary embodiment of circuit which provides the functions of the clock generator 420 of FIGURE 11. As illustrated in FIGURE 13, various portions of the circuit correspond to various components from the clock generator of FIGURE 11 with regard to function. However, in FIGURE 13, two PMOS transistors M17 and M18, as well as two NMOS transistors M11 and M12 operate in an unconventional configuration to provide the function provided by the conventional comparator 530 of FIGURE 11, as described in detail below. Likewise, two PMOS transistors M23 and M24, as well as two NMOS transistors M21 and M22 operate in an unconventional configuration to provide the function provided by the conventional comparator 540 of FIGURE 11, as described in detail below.

The ramp circuits 525 and 535 are also shown in FIGURE 13. As illustrated in FIGURE 13, the ramp circuit 525 includes a PMOS transistor M15, an NMOS transistor M10, as well as the capacitor C_{C2}. The ramp circuit 535 includes a PMOS transistor M19, an NMOS transistor M20, as well as the capacitor C_{C4}.

The logic circuit 550 is also shown in FIGURE 13. As illustrated, the logic circuit 550 includes five inverters U4, U5, U10, U11, and U12, as well as two OR gates U6 and U7, and a capacitor C_{C3}. Also illustrated in FIGURE 13 is an exemplary embodiment of a current setting circuit 515 that is integrally coupled to a comparator governing circuit 590 that is usable according to the systems and methods of this invention. The comparator governing circuit 590 (not shown in FIGURE 11) includes a PMOS transistor M13, as well as an NMOS transistor M9. As illustrated, the current setting circuit 515 is coupled to the comparator governing circuit 590 in a current mirror configuration. As shown, the resistor R_{C1} is connected to the power supply voltage VDD through PMOS transistor switch M3 and to the gate of NMOS transistor M8. Based on the operating characteristics of transistor M8, this configuration determines the threshold voltage V_{TH} at the circuit node connected to the gate of M8 as well as a current i_{C1} in the current setting circuit 515 which satisfies the condition $V_{TH} = VDD - (R_{C1} * i_{C1})$. As shown in FIGURE 13, the current i_{C1} is mirrored by the NMOS transistor M9. Thus the current flowing through PMOS transistor M13 of the comparator governing circuit 590, and which is connected to transistor M9, is also set at the level of the current i_{C1}. This current level programs the transistor M13 such that the gate voltage of the transistor M13 is set at a level corresponding to the current level of i_{C1} and the operating characteristics of the transistor type used for M13. As shown in FIGURE 13, the PMOS transistors M17 and M23, which are sized at two times the size of transistor M13, are connected to transistor M13 in a current mirror configuration and are thus programmed for a current level of $2* i_{C1}$. Furthermore, the NMOS transistor M11 which is connected to M17 is sized at two times the size of transistor M9, and is programmed by the current level of $2* i_{C1}$ established by M17. Based on the current density through transistor M11, transistor M11 is thus controlled to exhibit a gate threshold voltage of

V_{TH}. Transistor M11 thus effectively functions as the signal input of a comparator which switches at a threshold voltage V_{TH}. It should be appreciated that the transistors M23, M24, M21, and M22 of comparator 540 function identically to the corresponding transistors M17, M18, M11, and M12 of comparator 530.

As further shown in FIGURE 13, the PMOS transistors M10 and M20 which are sized at two times the size of transistor M8, are also connected to transistor M8 in a current mirror configuration and are thus programmed for a current level of 2* i_{C1}. The PMOS transistors M10 and M20, serve to determine the discharge currents i_{C2} and i_{C4} of capacitor C_{C2} and capacitor C_{C4}, respectively. Thus, in this exemplary embodiment of the clock circuit 420 of FIGURE 13, the discharge currents i_{C2} and i_{C4} respectively, are each controlled to be two times the current i_{C1} in the current setting circuit 515.

It should be appreciated that according to the foregoing discussion, the threshold voltage V_{TH} of each comparator is ultimately controlled based on a common signal which is determined by particular characteristics of the current setting circuit 515. This is a significant aspect of circuit operation in various embodiments according to the systems and methods of this invention, as described in greater detail below. Furthermore, given particular transistor sizes for the transistors M10 and M20, it should be appreciated that discharge currents i_{C2} and i_{C4} are also controlled based the common signal which determines V_{TH}, as determined by particular characteristics of the current setting circuit 515. This also is a significant aspect of circuit operation in various embodiments according to the systems and methods of this invention, as described in greater detail below.

Various other components are also shown in FIGURE 13, including a PMOS transistor M25, NMOS transistors M4 and M14, an inverter U14, and an OR gate U8. Transistors M25 and M4 in conjunction with inverter U10 and capacitor C_{C3} provide a delay for proper initialization of the clock when it is turned on.

The clock generator 420 shown in FIGURE 11 and the embodiment of the clock generator 420 shown in FIGURES 13 are each a dual ramp current-driven oscillator. With respect to FIGURE 13, since the capacitors C_{C2} and C_{C4} are

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discharged at a rate of $2i_{C1}$, governed by the current density mirroring of transistors M10 and M20 respectively, the discharge rate is:

$$\frac{dv}{dt} = \frac{2 \cdot i_{C1}}{C_C} = \frac{2 \cdot (VDD - V_{TH})}{R_{R1} \cdot C_C}$$

where $C_C = C_{C2}$ or C_{C4}, as appropriate.

5   Since the discharge will occur over the range from VDD to V_{TH}, the clock period will be given by:

$$T_{clk} = 2 \cdot \frac{VDD - V_{TH}}{\frac{dv}{dt}} = (R_{R1} C_C)$$

For example, with $R_{R1} = 2M\Omega$ and $C_C = 0.5PF$, $T_{clk} = 1uSec$.

10   Thus, it should be appreciated that the detailed circuit of Fig. 13 is a particularly simple and elegant way of implementing the circuit concepts described with respect to FIGURES 11-12, such that the clock frequency is substantially independent of variations in the supply voltage and transistor process parameters. In particular, through the mirroring techniques described above, the trip-point voltage for the comparators 530 and 540, and the discharge current which governs the clock

15   ramp signals in the comparators 530 and 540, are each controlled based on a common signal such that all voltage supply and transistor parameters variations become common mode factors which do not substantially affect the clock period during normal operation. Thus, the clock period depends only on the relevant resistor and

20   capacitors as described above.

In addition to the calculations for the clock generator components, it is also useful to examine the equations for the overall scale factor of an ADC according to the systems and methods of this invention. First of all, with regard to the exemplary current generator 410 of FIGURE 10, the charging rate of the single ramp signal of

25   an analog-to-digital converter, in various exemplary embodiments according to the systems and methods of this invention, is set by the bias circuit resistor R_R, the voltage level V_{REF}, and the ramp capacitor C_R.

The equation for calculating the related single ramp charging rate is shown below:

$$\left(\frac{dv}{dt}\right)_{ADC} = \frac{i_{R1}}{C_R} = \frac{V_{REF}}{(R_R C_R)}$$

If the exemplary clock circuit 420 of FIGURE 13 is then used in conjunction with the exemplary single ramp current generator 410, the overall ADC scale factor will be:

$$SF_{ADC}\left[\frac{counts}{Volt}\right] = \frac{1}{T_{clk} \cdot \left(\frac{dv}{dt}\right)_{ADC}} = \frac{1}{V_{REF}} \cdot \frac{(R_R C_R)}{(R_{C1} C_C)}$$

The relationship for the clock period, the single ramp charging rate, and the overall ADC scale factor, as shown by the above equations, has two important benefits. First, if the clock resistors and capacitors and the ADC ramp signal generator resistors and capacitors are constructed in a similar manner within a single integrated circuit, the device characteristics will generally match proportionally and the scale factor will be independent of process variations during fabrication. Furthermore, it should be appreciated the scale factor will be significantly independent of environmental variations when the circuit is operating, because the device operating characteristics that determined the scale factor are generally also matched proportionally according to the device design and fabrication, as described above.

Second, since the transducer signal will be proportional to the supply voltage, by deriving V_{REF} directly from the overall system power supply (using a divider), the system's scale factor (peak-to-peak counts for each differential signal from the transducer) will be made to be independent of the system supply voltage variations. Thus, all voltage supply variations, transistor parameters variations, and passive component parameter variations become common mode factors which do not substantially affect the overall measurement accuracy of circuits constructed according to the systems and methods of the invention, as described above.

Another consideration for the overall system of the present invention is the signal droop in the analog-to-digital converter. Since the input signal is stored in the input capacitor of the comparator during conversion, the leakage currents in the comparator switches will cause signal droop in the analog-to-digital converter.

5   Leakage currents in the bias circuit can alter the charging rate and the scale factor of the analog-to-digital converter. As is known in the art, there are at least two causes of leakage currents in an MOS transistor. The first cause may be referred to as drain/source P-N junction reverse currents. The second cause may be referred to as sub-threshold conduction, whereby if V_{GS} is close to zero or slightly below zero, the

10   sub-threshold drain current can be as much as the D/S junction leakage (or more). Using non-minimum length MOS switches reduces sub-threshold conduction.

The analog-to-digital converter of the present invention has a number of advantages with regard to the effects of leakage currents. One advantage is that the effect of leakage in the analog-to-digital converter comparators will be canceled, since the design is fully differential in nature. In addition, while voltage dependent

15   leakage in general will introduce second order distortion, the fully differential nature of the present invention effectively transforms such second order distortion into third order distortion and will thus not introduce position errors when the analog-to-digital converter is used in conjunction with a three-phase transducer system such as that

20   described above.

With regard to specific circuit characteristics achievable according to the present invention, in one exemplary embodiment of a six-channel ADC (six fully differential pairs) according to the systems and methods of this invention, suitable for use in conjunction with 1.5V power supply and a three-phase transducer such as that

25   described above, the average current consumption was approximately 0.8 microamperes and the exemplary ADC could be implemented in an area of approximately 0.8 square millimeters according to a conventional silicon IC layout.

FIGURE 14 illustrates one embodiment of an overall measuring system 600 in accordance with the present invention. Continuing to use the exemplary input

30   provided by a three-phase position transducer, as illustrated, an input multiplexer 610

receives inputs from scales A, B, and C, as well as reference signals REF0 and REF1. The three outputs of the multiplexer 610 are provided to three pre-amplifiers 620-622. The three outputs of the three amplifiers 620-622 are provided to a channel multiplexer 630. The channel multiplexer 630 provides six outputs to

5   six integrator stages 640-645. The outputs of each of the integrator stages 640-645 are each provided to a channel 660-665 of a 6-channel analog-to digital converter. The 6-channel analog-to-digital converter receives a ramp signal from a ramp generator 650. The outputs of the six channels are output signals OUT0-OUT5, which are three phase-related measurements for each of two scales.

10   The embodiment of the measurement system 600 of FIGURE 14 is very power efficient. The pre-amps 620-622 are BiCMOS pre-amplifiers. The system is designed to perform mismatch error correction, in that the input multiplexer 610 receives inputs for two on-chip references, including the zero signal REF0 for offset correction, and a full scale reference signal REF1 for gain mismatch correction. In

15   one embodiment, one cycle per second is used for error correction (alternating between the signals REF0 and REF1).

FIGURE 15 is a timing diagram illustrating the operation of the measuring system 600 of FIGURE 14. As illustrated in FIGURE 15, the scale A and B samples are centered on the same point in time (384uS). This ensures minimum speed-

20   induced errors for position computations using the input provided by the exemplary three-phase position transducer. For each display update, one set of two scales are sampled: A and B, or A and C, for reason as described in the references incorporated herein.

It should be appreciated that all or part of the circuits described with regard to

25   FIGURES 6-15 are suitable for combined fabrication in a single integrated circuit, which may furthermore include at least some of the circuits described with regard to FIGURE 2. Furthermore, while the circuits described with regard to FIGURES 6-15 are particularly advantageous for low power low voltage operation, it should be appreciated that circuits according to the systems and methods of this invention

30   retain advantages when fabricated to operate at higher voltage levels. Furthermore,

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circuits implementations according to the systems and methods of this invention which are operable from a low voltage power supply at lower voltage levels, such as 1.35 volts, 1.5 volts, 3 volts, or 3.5 volts, for example, are also typically able to operate at voltage levels at least three to fives times higher, limited only by the

5   voltage limitations of the processes used to fabricate the circuits. Furthermore, a number of the concepts and circuit portion described herein are advantageously usable both separately and in various combinations, thus, while the preferred embodiment and a limited number of other exemplary embodiments and variations of the invention have been illustrated and described, it will be appreciated that various

10   changes can be made therein without departing from the spirit and scope of the invention.